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NXP, B.V.
NXP INTELLECTUAL PROPERTY & LICENSING
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
GILES, EBONI N	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/564,293
Filing Date: January 10, 2006
Appellant(s): WETZKER ET AL.

Terry W. Kramer
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 1 October 2009 appealing from the Office action mailed 5 June 2009.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments

The appellant's statement of the status of amendments contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

2004/0057534	MASENTEN	3-2004
20040210801	PRASAD	10-2004
20040032355	MELANSON	2-2004

6225928	GREEN	5-2001
7130327	ROBINSON	10-2006

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication 2004/0057534 to Masenten et al. ("Masenten") in view of U.S. Patent Publication 2004/0210801 to Prasad et al ("Prasad").

Regarding Claim 1, Masenten discloses "a receiver comprising a receiving stage that receives frequency signals; a mixing stage coupled to the receiving stage that generates converted frequency signals, a modulating stage coupled to the mixing stage that delta-sigma modulates the converted frequency signals; a filtering stage coupled to the modulating stage that filters the delta-sigma modulated converted frequency signals," where, in a third embodiment, the receiver includes an integrated low noise amplifier (LNA) which may utilize one broadband or multiple narrow band low noise amplifiers for amplifying received RF signals…The output of the active LNA is inputted to an in-phase (I)-path

mixer and quadrature (Q)-path mixer, each of whose function is to translate the center frequency of the desired RF signal by a local oscillator frequency, f_{LO}, to an intermediate frequency, f_{IF} (¶0030, Fig. 3, elements 10, 110, 120A, 120B) and further discloses in a fourth embodiment where the output of each mixer is coupled to a delta-sigma modulator respectively through Node 1. Node 1 is implemented as an IF filter that provide both a tuned output for the corresponding mixer and a bandpass centered at the IF frequency for the first stage of the corresponding delta-sigma modulator (¶ 0029, 0034, Fig. 4a, elements 120A, 120B, 130A, 130B, 140A, 140B).

Masenten does not expressly disclose "wherein the filtering stage comprises a decimator receiving an output signal from a time-control loop having a loop quantizer and a loop filter.

Prasad teaches a delta-sigma analog-to-digital converter (ADC) where each delta-sigma modulator comprises a summer, low pass filter, quantizer and DAC in a delta-sigma feedback loop. The outputs from the delta-sigma modulators are each passed through a digital decimation filter which reduces the sample rate. Delta-sigma modulators sample the analog input signals at an oversampling rate and output digital data based on the quantization at the oversampling rate (¶ 0014-0016, Fig. 1, elements 100, 102, 104, 105, 106, 107). The delta-sigma feedback loop would be operable as the claimed timing control loop since it adjusts the re-sampling instants of the ADC.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the receiver of Masenten with the decimation filter of Prasad. The suggestion/motivation would have been in order to acquire and track the timing of a given signal instance.

Regarding Claim 2, Masenten and Prasad disclose a receiver as recited in Claim 1 and further discloses that the modulating stage comprises a delta-sigma modulator comprising a low-pass filter; a quantizer coupled to the low-pass filter; and a digital-to-analog converter for feeding back an output of the quantizer to an input of the low-pass filter," where the output of each delta-sigma modulators is coupled to a decimation filter. Each decimation filter filters and decimates the output signal from the respective delta-sigma modulator to forma high resolution digital signal at a sampling rate where MD is the decimation ratio of the decimation filter. The decimation filter divides down the sampling rate of the digital signal by MD. Each decimation filter has a lowpass frequency response (¶ 0036-0038, Fig 6A-6C, elements 140A, 140B, 150A, 150B).

Regarding Claim 5, Masenten and Prasad disclose a receiver as recited in Clam 1 and Masenten further discloses that "the mixing stage comprises a mixer and the modulating stage comprises a delta-sigma modulator," where the mixers decompose the received signal into in-phase and quadrature phase components. The I mixer outputs the in-phase component of the received signal at the IF and the Q mixer outputs the quadrature component of the received signal at the IF (¶ 0032, Fig. 4a, elements 120A and 120B) and further discloses that the delta-

sigma modulator includes a lowpass filter for a follow-on Node within the delta-sigma modulator. The bandpass filters of Node 1 and the lowpass filter for the follow-on Node result in both a signal transfer function (STF) and noise transfer function with a bandpass transfer function centered at the IF frequency. This provides rejection of DC and 1/f noise components from the respective mixer and also provides IF pre-filtering to attenuate signals outside of the channel bandwidth of the desired signal (¶ 0035, Fig. 4a, elements 140A, 140B).

Regarding Claim 6, Masenten and Prasad disclose a receiver as recited in Claim 1 and Masenten further discloses in a fifth embodiment that the receiver may utilize one broadband DLNA to amplify both frequency bands…the differential output of the DLNA is coupled to both the in-phase mixer and the quadrature mixer. The in-phase mixer receives a differential in-phase local oscillator signal and the quadrature mixer receives a differential quadrature local oscillator signal from the clock generation and distribution circuit. The output of the I mixer is coupled to the I delta-sigma modulator via the I-path IF filter and the output of the mixer is coupled to the Q delta-sigma modulator via the Q-path IF filter (¶ 0046, Fig. 5, elements 110, 120A, 120B, 122B, 130A, 130B, 140A, 140B).

Regarding Claim 7, Masenten discloses "a system comprising a transmitter and a receiver," where high frequency signals are received through an antenna and inputted to a duplexer…The duplexer couples the receive signal to the receiver and couples transmit signals from the transmitter to the antenna (¶

0026, Fig. 1, elements 10, 20, 22, 23, 25). The receiver is drawn to the apparatus recited in Claim 1 as taught by Masenten and Prasad and rejected for the same reasons of obviousness above.

Process claim 8 is drawn to the method of using the corresponding apparatus claimed in claim 1. Therefore, process claim 8 corresponds to apparatus claim 1and is rejected for the same reasons of obviousness above.

As to Claim 9, they are rejected for the same reasons indicated above because they recite similar limitations claimed in Claim 1.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Pub. 2004/0057534 to Masenten et al. ("Masenten") in view of U.S. Patent Publication 2004/0210801 to Prasad et al ("Prasad") as applied to claim 2 above and in view of US Patent 7,194,036 to Melanson.

Regarding Claim 3, Masenten and Prasad disclose a receiver as recited in Claim 2.

Masenten and Prasad do not expressly disclose that the low-pass filter comprises a time-continuous filter.

Melanson discloses that "the low-pass filter comprises a time-continuous filter," where the first delta-sigma modulator has a low-pass STF (signal transfer function) defined by a complex set of poles (Col. 6, lines 15-16) where a signal transfer function with a set of poles is indicative of a time-continuous filter.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Pub. 2004/0057534 to Masenten et al. ("Masenten") in view of U.S. Patent

Publication 2004/0210801 to Prasad et al ("Prasad") as applied to claim 1 above and in further view of US Patent 7,130,327 to Robinson et al. ("Robinson").

Regarding Claim 4, Masenten and Prasad disclose a receiver as recited in Claim 1.

Masenten and Prasad do not expressly disclose a further mixing and filtering stage.

Robinson does expressly disclose "a further mixing stage coupled to the filtering stage for generating baseband signals; and a further filtering stage coupled to the further mixing stage for channel selective filtering the baseband signals," where the filter is operative to mitigate quantization noise and noise that has been shifted or shaped to out-of-band frequencies by the delta-sigma modulation implemented by the modulator. The filter output signal can be passed to an amplifier operative to amplify the selected signal pattern to provide an output signal at a desired level. The amplified signal can be provided as a local oscillator signal to drive a mixer such that the signal operates as a carrier frequency for transmission of wireless communication signals or for up or down conversion in a transceiver (Col. 8, lines 18-28).

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Pub. 2004/0057534 to Masenten et al. ("Masenten") in view of U.S. Patent Publication 2004/0210801 to Prasad et al ("Prasad") as applied to claim 1 above and in view of U.S. Patent 6,225,928 to Green.

Regarding Claim 11, Masenten and Prasad disclose a receiver as recited in Claim 1.

Masenten and Prasad do not expressly disclose an adder, an inverse z block or a gain block.

Green teaches that the loop filter further comprises: an adder that combines a detected signal with a feedback signal, thereby producing a sum; an inverse z block that receives the sum and produces a feedback signal; a gain block that processes the feedback signal (Col. 5, line 66 – Col. 6, line 34, Fig. 3, elements 206, 220, 222, 310, 312, 314, 316, 318, 320, 322, 324) where a delta-sigma ADC is described that comprises a complex bandpass loop filter with a transfer function, H(z). The in-phase and quadrature signals are received by the adder which subtracts them from a feedback signal. The output signals are provided to the complex loop filter for quantization. The in-phase and quadrature phase signals having a desired gain generate a feedback signal. The quantization noise is removed by passing it through decimation filters subsequent to the ADC. Green further discloses producing the output signal that is sent to the loop quantizer to control the decimator (Col. 13, lines 34-57, Fig. 10, elements 208, 1014, 1020, 1022, 1028, 1032, 1036, 1040) where the power estimation circuitry receives real (I) and imaginary (Q) output signals from the decimation filters, control circuitry receives power estimation signal and produces gain control signals which respectively control input and output variable gain blocks located in the ADC input and output imaginary paths.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the receiver of Masenten and Prasad with the loop filter of Green. The suggestion/motivation would have been in order to automatically detect and compensate for mismatches in the delta-sigma ADC (Col. 13, lines 34-35).

(10) Response to Argument

In section "A" (i.e. page, 6, item "1") appellants assert that claims 1, 7, 8 and 9 are not disclosed in the prior art of record with respect to 35 USC 103(a) over Masenten in view of Prasad.

The examiner asserts that the argument is not persuasive. As explained in the Final office action, Masenten (U.S. Patent Application 2004/0057534) teaches, in the same field of endeavor, a complex-IF digital receiver. The receiver receives RF signals from a LNA (low noise amplifier) (i.e. receiving stage) and provides them to an I-path mixer and a Q-path mixer. Masenten further discloses the claimed mixing stage where the mixers translate the center frequency of the desired RF signal by a local oscillator frequency, fLO, to an intermediate frequency, Fif (i.e. converted frequency signals) using a VCO (voltage controlled oscillator) (¶ 0030, Fig. 3: 110, 120A, 120B, 130A, 130B). Masenten further discloses the claimed modulating stage as the output of each mixer is coupled to a delta-sigma (ΔΣ) modulator (¶ 0036, Fig. 3: 130A, 130B, 140A, 140B). Each delta-sigma modulator for the respective I/Q paths are identical and converts the input signal at the IF filter into an output stream at a

particular sampling rate. Masenten further discloses the claimed filtering stage where a decimation filter for each path (i.e. I/Q) filters and decimates the output signal from the respective delta-sigma modulator (¶ 0037, Fig. 3: 140A, 140B, 150A, 150B). The appellant reveals the receiving stage (Fig. 2: 12), mixing stage (Fig. 2: 13), modulating stage (Fig. 2: 14) and filtering stage (Fig. 2: 15) on pages 6 and 7 of the disclosure.

The appellant further asserts that the limitation "wherein the filtering stage further comprises a decimator receiving a feedback signal from a time-control loop having a loop quantizer and a loop filter" is not disclosed with respect to 35 USC 103(a) over Masenten in view of Prasad. The Examiner asserts that the argument is not persuasive. As stated in the Final rejection, Masenten fails to disclose a filtering stage comprising a decimator receiving an output signal from a time-control loop having a loop quantizer and a loop filter. Therefore, Masenten's delta-sigma modulator and decimation filter would be replaced by the corresponding components in the Prasad reference. Prasad (U.S. Patent Application 2004/0210801) teaches a ΔΣ-ADC (delta-sigma analog-to-digital converter) (Fig. 1: 100) which comprises a delta-sigma modulator (Fig. 1: 102) with a feedback loop (i.e. time-control loop) comprising a comparator (i.e. loop quantizer) (Fig. 1: 105), a low pass filter (i.e. loop filter) (Fig. 1: 104) and a DAC (i.e. digital-to-analog converter) (Fig. 1: 106). This particular arrangement of a ΔΣ modulating stage comprising a time-control loop is identical to Figure 3, page 8 of the appellant's disclosure. The ΔΣ modulator of Prasad uses a feedback

loop to sample the corresponding analog input signals at an over-sampling rate hence it is utilized as a time-control loop.

The appellant further asserts that Prasad does not have a feedback loop from a detector going back to the decimator through a loop filter and a quantizer. The Examiner disagrees as the appellant correctly asserts that the decimation filter feeds forward a signal to a LPF (Fig. 1: 108). The LPF that the appellant relies upon is not the recited loop filter; rather it is depicted as the LPF within the ΔΣ modulator (Fig. 1: 104). The recited feedback loop is disclosed within the ΔΣ modulator of Prasad (Fig. 1: 102). The recited loop filter and quantizer, as previously stated, are disclosed within the ΔΣ modulator of Prasad. Furthermore, the ΔΣ modulator of Prasad uses its feedback signal as an output to a digital decimation filter (Fig. 1: 107) (i.e. decimator). The digital decimation filter (i.e. decimator) should be used in the filtering stage, Figure 3 of applicant's disclosure does not include the decimation filter in the feedback loop but rather feeds forward the output of the ΔΣ modulating stage to the filtering stage by way of the decimator in Figure 2 and page 7, lines 9-13 of his claimed invention.

The appellant further asserts that the loop quantizer is not present. The Examiner disagrees as the appellant incorrectly asserts that the DAC is being represented as the claimed loop quantizer. Prasad teaches the use of a comparator as a quantizer (¶ 0016, Fig. 1: 105) which feeds back its signal to a DAC (digital-to-analog converter) in the loop.

The appellant further asserts that the Prasad reference lacks a loop filter. The Examiner disagrees as the appellant incorrectly asserts that the DAC is the only element of the feedback loop in the Prasad reference. Prasad teaches a low pass filter (Fig. 1: 104) embodied within the ΔΣ modulator that feeds forward a signal to the quantizer (i.e. comparator in Prasad) whose output is fed back through a DAC.

Therefore, in view of the examiner, a combination of Masenten and Prasad teaches every limitation claimed by appellant with regard to Claims 1, 7, 8 and 9.

In section "A", item 2, the appellant argues that claims 2, 5 and 6 are not obvious over Masenten in view of Prasad since each depends upon claim 1. The examiner provides the same argument as in the above response to appellant's argument of Claim 1.

In section "B", the appellant argues that claim 3 is not obvious over Masenten in view of Prasad in view of Melanson and that Melanson does not cure the deficiencies of Masenten and Prasad with regard to the time-control loop of Claim 1. The Examiner agrees that Melanson does not disclose a feedback signal to a decimator and also lacks a time-control loop having a loop quantizer and loop filter. The examiner relies upon the Prasad reference used in the 35 U.S.C. 103(a) rejection of Claims 1, 7, 8 and 9 to teach the recited time control loop having a loop quantizer and loop filter. Therefore, the Examiner provides

the same argument as in the above response to appellant's argument of Claims 1, 7, 8 and 9.

In section "C",the appellant argues that claim 4 is not obvious over Masenten in view of Prasad in view of Robinson and that Robinson does not cure the deficiencies of Masenten and Prasad with regard to the time-control loop of Claim 1. The Examiner agrees that Robinson does not disclose a feedback signal to a decimator and also lacks a time-control loop having a loop quantizer and loop filter. The examiner relies upon the Prasad reference used in the 35 U.S.C. 103(a) rejection of Claims 1, 7, 8 and 9 to teach the recited time control loop having a loop quantizer and loop filter. The examiner provides the same argument as in the above response to appellant's argument of Claim 1.

In section "D", the appellant asserts that claim11 is not disclosed in the prior art of record with respect to 35 USC 103(a) over Masenten in view of Prasad in further view of Green.

The appellant asserts that the loop filter comprising an adder, inverse z block and a gain block are absent from Masenten in view of Prasad in further view of Green. The examiner asserts that the argument is not persuasive. The Examiner concedes that Masenten or Prasad, alone or in combination, do not teach the claimed adder, inverse z block or gain block. As explained in the final office action, Green (U.S. Patent 6,225,928) teaches a ΔΣ-ADC (delta-sigma analog-to-digital converter) comprising a complex loop filter (Col. 5, line 65 – Col. 6, line 22, Fig. 3: 206, 300). The two adders receive both in-phase and

quadrature phase signals respectively and subtracts from each in-phase/quadrature phase signal a respective feedback signal (Fig. 3: 220, 222, 310, 312, 322, 324). The adder sums the resulting into respective in-phase and quadrature phase signals (Fig. 3: 314, 316). Green further teaches the claimed gain block where a feedback loop passes the in-phase/quadrature phase digital signals to a DAC having a desired gain to generate a feedback signal which is passed through the loop filter and quantizer (Fig. 3: 224, 226, 308, 322). The claimed inverse z block is disclosed as an embodiment of the complex loop filter (Col. 8, lines 30-45, Fig. 6). The input signals, I_1, I_2 (i.e. in-phase/quadrature phase signals) are received and passed through a delay block z^{-1} (i.e. inverse z block) to provide a feedback signal to the output, O_1, O_2 (Fig. 6: 602, 604, 626).

The appellant asserts that the loop filter does not produce an output signal sent to a loop quantizer to control a decimator. The Examiner asserts that the argument is not persuasive. The digital output of the ΔΣ-ADC taught by Green as referred to in the above argument is passed through digital decimation filters (Col. 5, lines 24-26, Fig. 2: 206, 208).

The appellant asserts that the adder, inverse z block and gain block are not recited in the context of a loop filter. The Examiner asserts that the argument is not persuasive. The ΔΣ-ADC (delta-sigma analog-to-digital converter) cited in the above argument comprises a complex loop filter (Fig. 3: 206, 224, 226, 300, 308, 322; Fig. 6). The examiner provides the same argument as in the above

response to appellant's argument that the elements are not present in the Green reference.

The appellant asserts that the adder, inverse z block and gain block are not comprised within the loop filter. The Examiner asserts that the argument is not persuasive. The ΔΣ-ADC (delta-sigma analog-to-digital converter) cited in the above argument is used to shape quantization noise which is a well-known purpose of a filter in the art. The above argument states that each of the elements taught by Green is comprised within the ΔΣ-ADC (delta-sigma analog-to-digital converter) (Fig. 3: 206, 224, 226, 300, 308, 322; Fig. 6). Therefore, the examiner provides the same argument as in the above response to appellant's argument that the elements are not present in the Green reference.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/ EBONI GILES/

Examiner, Art Unit 2611

Conferees:

/Mohammad H Ghayour/

Supervisory Patent Examiner, Art Unit 2611

/CHIEH M FAN/

Supervisory Patent Examiner, Art Unit 2611